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Applicant	James Leroy Snell	**SUPPLEMENTAL PRELIMINARY AMENDMENT**
Serial No.	10/005,483	
Filing Date	November 9, 2001	
Group Art Unit	2631	
Examiner Name	Unknown	
Attorney Docket No.	125.003USR1	
Title: HIGH DATA RATE SPREAD SPECTRUM TRANSCEIVER AND ASSOCIATED METHODS		

Commissioner for Patents
Washington, D.C. 20231

Prior to initial review, please add the following new claims:

IN THE CLAIMS

123. (New) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence generated at a predetermined chip rate;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by selecting for each of said N-bit second data symbols one of a set of 2^N chip sequences generated at the same chip rate as said spreading sequence; and

applying the spread-spectrum encoded symbols of said header field and the selected chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

124. (New) The method of claim 123 wherein each said chip sequence is selected in accordance with a first data segment of an N-bit second data symbol and is differentially phase encoded in accordance with a second data segment of the same N-bit second data symbol.

125. (New) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by selecting for each of said N-bit second data symbols one of a set of 2^N chip sequences, each of said selected chip sequences being differentially phase encoded;

applying a reference phase based on encoding of the last of said first data symbols to the differential encoding of the first selected chip sequence; and

inputting said encoded symbols of said header field and said differentially encoded chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

126. (New) The method of claim 125 wherein each said chip sequence is selected in accordance with a first data segment of an N-bit second data symbol and is

differentially phase encoded in accordance with a second data segment of the same N-bit second data symbol.

127. (New) A method of generating an rf signal in a transmitter having a phase shift modulator with I and Q inputs comprising the steps of:

supplying a stream of binary information containing header data and payload data, said header data specifying at least a first payload data rate or a second payload data rate;

encoding said payload data when said header data specifies said first payload data rate by grouping said payload data into N-bit symbols, where N is greater than 1, and applying each N-bit symbol to select one of 2^N possible chip sequences;

encoding said payload data when said header data specifies said second payload data rate by grouping said payload data into 2N-bit symbols and applying each 2N-bit symbol to select one of 2^{2N} possible chip sequences; and

applying each selected chip sequence to the I and Q inputs of said phase shift modulator.

128. (New) The method of claim 127 wherein the chip sequences selectable by said 2N-bit symbols include the chip sequences selectable by said N-bit symbols plus 2^{2N}-2^N additional chip sequences.

129. (New) The method of claim 127 wherein the chip sequences selected by said N-bit symbols and said 2N-bit symbols are generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit or 2N-bit symbol and

differentially phase encoding the selected initial chip sequence in accordance with a second data segment of the same N-bit or 2N-bit symbol.

130. (New) The method of claim 127 wherein each of the 2^{2N} chip sequences selectable by said 2N-bit symbols comprises an I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively.

131. (New) The method of claim 129 wherein N=4 and wherein each chip sequence selected by a 2N-bit symbol comprises an initial I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively, said initial I/Q chip sequence being selected by 6 bits of a 2N-bit symbol and being differentially phase encoded in accordance with the other 2 bits of the same 2N-bit symbol.